[0209] The RAID storage system **2000** may include the RAID controller **2500**. The RAID controller **2500** may include the RAID controller **100** of FIG. **6**. The RAID controller **2500** may operate according to at least some example embodiments of the inventive concepts described with reference to FIGS. **7** through **17**.

[0210] For example, the RAID controller **2500** may manage information of ECC result indicators, based on results of ECC decoding operations received from the ECC circuits **2111***a*, **2111***b*, and **2111***c*. The RAID controller **2500** may recover a data chunk that includes ECC unit data having an uncorrectable ECC error, with reference to the ECC result indicators. The RAID controller **2500** may provide a host with a stripe including the recovered data chunk. For brevity, some redundant descriptions will be omitted from the description of FIG. **18**.

[0211] As illustrated in FIG. **18**, the RAID controller **2500** may be implemented in an independent circuit or device. Alternatively, some or all of functions of the RAID controller **2500** may be included in the central controller **2300**, or may be distributed to the device controllers **2110***a*, **2110***b*, and **2110***c*.

[0212] The RAID controller **2500** may support a multi-channel communication according to the number of the storage devices **2100***a*, **2100***b*, and **2100***c*. According to at least some example embodiments of the inventive concepts, the RAID controller **2500** may be implemented by separate circuits or devices as much as the number of the storage devices **2100***a*, **2100***b*, and **2100***c*. According to at least some example embodiments of the inventive concepts, the ECC circuits **2111***a*, **2111***b*, and **2111***c* may be implemented in one circuit or device, and thus may be configured to correspond to one RAID controller **2500**.

[0213] As described above, the RAID controller **2500** may include several memory regions. However, according to at least some example embodiments of the inventive concepts, the RAID controller **2500** may share a memory region of the host and/or the storage devices **2100***a*, **2100***b*, and **2100***c*. At least some example embodiments of the inventive concepts may be variously changed or modified.

[0214] FIG. **19** is a block diagram illustrating a storage device that includes a RAID controller in accordance with at least some example embodiments of the inventive concepts.

[0215] According to at least some example embodiments of the inventive concepts, the RAID storage device **1200** of FIG. **1** may be implemented in one storage device **3000**. The storage device **3000** may include a plurality of nonvolatile memory devices **3100**. The nonvolatile memory devices **3100** may dispersively store a plurality of data chunks and a parity included in one stripe. The nonvolatile memory devices **3100** may include a nonvolatile memory examples of which include, but are not limited to, a flash memory, a PRAM, a ReRAM, a MRAM, and/or a FRAM.

[0216] The storage device **3000** may include a device controller **3300**. The device controller **3300** may control the overall operations of the storage device **3000**. For example, the device controller **3300** may include one or more ECC circuits **3310**. The ECC circuits **3310** may perform. ECC decoding operations on a plurality of ECC unit data included in the stored data chunk(s).

[0217] The device controller **3300** may include the RAID controller **3330**. The RAID controller **3330** may include the RAID controller **100** of FIG. **6**. The RAID controller **3330** may operate according to at least some example embodiments of the inventive concepts described with reference to FIGS. **7** through **17**

[0218] For example, The RAID controller **3330** may manage information of ECC result indicators, based on results of ECC decoding operations received from the ECC circuits **3310**. The RAIL) controller **3330** may recover a data chunk that includes ECC unit data having an uncorrectable ECC error, with reference to the ECC result indicators. The RAID controller **3330** may provide a host with a stripe including the recovered data chunk. For brevity, redundant descriptions will be omitted.

[0219] As illustrated in FIG. **19**, the RAID controller **3330** may be included in the device controller **3300**. Alternatively, the RAID controller **3330** may be configured separately from the device controller **3300**, or may be configured separately from the storage device **3000**.

[0220] The RAID controller **3330** may support a multi--channel communication according to the number of the nonvolatile memory devices **3100**. According to at least some example embodiments of the inventive concepts, the RAIL) controller **3330** may be implemented by separate circuits as much as the number of the nonvolatile memory devices **3100**. According to at least some example embodiments of the inventive concepts, the ECC circuits **3310** may be implemented by separate circuits as much as the number of channels being supported by the RAID controller **3330** or as much as the number of the nonvolatile memory devices **3100**.

[0221] As described above, the RAID controller **3330** may include several memory regions. However, According to at least some example embodiments of the inventive concepts, the RAID controller **3330** may share a memory region of the host, the device controller **3300**, and/or the storage device **3000**. At least some example embodiments of the inventive concepts may be variously changed or modified.

[0222] According to at least some example embodiments of the inventive concepts, a data chunk including an uncorrectable error may be recovered. Thus, the RAID storage system or the storage device may guarantee high reliability of data. Furthermore, the RAID storage controller may not require additional parity to recover a data chunk. Thus, the overhead of the RAID storage system or the storage device may not greatly increase.

[0223] Circuits, chips, and devices according to at least some example embodiments of the inventive concepts may be mounted using various kinds of semiconductor packages. For example, circuits, chips, and devices according to at least some example embodiments of the inventive concepts may be mounted using a package such as package on package (PoP), bail grid arrays (BGAs), chip scale packages (CSPs), plastic leaded chip carrier (PLCC), plastic dual in-line package (PDIP), die in. waffle pack, die in wafer form, chip on board (COB), ceramic dual in-line package (CERDIP), metric quad flat pack (MQFP), small outline integrated circuit (SOIC), shrink small outline package (SSOP), thin small outline package (TSOP), thin quad flat pack (TQFP), system in package (SIP), multi-chip package (MCP), wafer-level fabricated package (WFP),and/or wafer-level processed stack package (WSP).

[0224] Example embodiments of the inventive concepts having thus been described, it will be obvious that the same may be varied in. many ways. Such variations are not to be regarded as a departure from the intended spirit and scope of